WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of word lines formed along a first direction;

a plurality of bit lines formed along a second direction crossing at right angles to the first direction;

a first memory cell including a magneto-resistive element which has either a first resistance or a second resistance smaller than the first resistance;

a second memory cell including a magneto-resistive element which has a resistance between the first and second resistances;

a memory cell array including the first and second memory cells disposed in intersections of the word line and bit line;

a row decoder which selects the word line;

a row driver which supplies a first write current to the word line selected by the row decoder;

a column decoder which selects the bit line;

a column driver which supplies a second write current to the bit line selected by the column decoder; and

a sense amplifier which amplifies data read from the first memory cell selected by the row decoder and column decoder.

2. The device according to claim 1, wherein the

current value of the first write current supplied by the row driver is variable in accordance with the word line.

3. The device according to claim 1, wherein the row driver comprises a first current source which supplies the first write current and a second current source which supplies the first write current smaller than the current supplied by the first current source.

4. The device according to claim 3, wherein the first current source supplies the first write current to the word line such that the magneto-resistive element of the first memory cell has either the first or second resistance to perform write operation, and

the second current source supplies the first write current to the word line such that the magneto-resistive element of the second memory cell has a resistance between the first and second resistances.

5. The device according to claim 4, further comprising:

a hold circuit which holds the value of the first write current required to set the resistance of the magneto-resistive element of the second memory cell to a value between the first and second resistances.

6. The device according to claim 1, wherein the current value of the second write current supplied by the column driver is variable in accordance with the bit line.

7. The device according to claim 6, wherein the column driver supplies the second write current to the bit line such that the magneto-resistive element of the first memory cell has either the first or second resistances to perform write operation, and

the column driver supplies the second write current to the bit line such that the magneto-resistive element of the second memory cell has a resistance between the first and second resistances.

8. The device according to claim 7, further comprising:

a hold circuit which holds the value of the second write current required to set the resistance of the magneto-resistive element of the second memory cell to a value between the first and second resistances.

9. The device according to claim 1, wherein the second memory cells are arranged at the intersection of any one bit line and word lines.

10. The device according to claim 1, wherein the sense amplifier amplifies the data read from the first memory cell based on the data held by the second memory cell.

11. The device according to claim 10, wherein the sense amplifier identifies the data read from the first memory cell by a magnitude with respect to the data read from the second memory cell.

12. The device according to claim 1, further

comprising:

a judgment circuit to judge whether or not the resistance of the magneto-resistive element of the second memory cell is in a predetermined range between the first and second resistances; and

a control circuit to command the rewriting of the data with respect to the second memory cell, when the resistance of the magneto-resistive element of the second memory cell is not in a predetermined range as a result of judgment in the judgment circuit.

13. The device according to claim 12, wherein the control circuit controls the value of the current supplied by either one of the row driver and column driver in accordance with a judgment result in the judgment circuit in commanding the rewriting.

14. A semiconductor memory device comprising:

a plurality of word lines formed along a first direction;

a plurality of bit lines formed along a second direction crossing at right angles to the first direction;

a memory cell including a magneto-resistive element;

a memory cell array including the memory cells disposed in an intersection of the word line and bit line;

a row decoder which selects the word line;

a column decoder which selects the bit line;

a driver circuit which supplies write currents to the word line and bit line selected by the row decoder and column decoder, respectively and in which a current value of the write current is variable in accordance with the word line or bit line; and

a sense amplifier which amplifies data read from the memory cell selected by the row decoder and column decoder.

15. The device according to claim 14, wherein the driver circuit comprises a first current source provided for the word lines, and a second current source provided for the word lines and having a greater current drive ability than the first current source.

16. The device according to claim 15, wherein the second current source supplies the write current to the word line such that the magneto-resistive element of the memory cell has either a first resistance or a second resistance smaller than the first resistance to perform write operation, and

the first current source supplies the write current to the word line such that the magneto-resistive element of the memory cell has a resistance between the first and second resistances.

17. The device according to claim 16, wherein the memory cells having the resistance between the first and second resistances are arranged at intersections of

any one bit line and word lines.

18. The device according to claim 16, wherein the sense amplifier amplifies the data read from the memory cell having either the first or second resistance based on the data held by the memory cell which has a resistance between the first and second resistances.

19. The device according to claim 18, wherein the sense amplifier identifies the data read from the memory cell having either the first or second resistance by a magnitude with respect to the data read from the memory cell which has the resistance between the first and second resistances.

20. The device according to claim 16, further comprising:

a hold circuit which holds the value of the write current required to set the resistance of the magneto-resistive element of the memory cell to a value between the first and second resistances.

21. The device according to claim 16, further comprising:

a judgment circuit to judge whether or not the resistance of the magneto-resistive element of the memory cell is in a predetermined range between the first and second resistances; and

a control circuit to command the rewriting of the data with respect to the memory cell, when the resistance of the magneto-resistive element of the

memory cell is not in the predetermined range as a result of judgment in the judgment circuit.

22. The device according to claim 21, wherein the control circuit controls the value of the current supplied by the driver circuit in accordance with a judgment result in the judgment circuit in commanding the rewriting.

23. The device according to claim 14, wherein the driver circuit supplies the write current to the bit line such that the magneto-resistive elements of the memory cells arranged at the intersections of the word lines and some of the bit lines have either a first resistance or a second resistance smaller than the first resistance to perform write operation, and the driver circuit supplies the write current to the bit line such that the magneto-resistive elements of the memory cells arranged at the intersections of the word lines and the remaining bit lines have a resistance intermediate between the first and second resistances.

24. The device according to claim 23, wherein the memory cells having the resistance between the first and second resistances are disposed in an intersection of any one bit line and word lines.

25. The device according to claim 24, wherein the sense amplifier amplifies the data read from the memory cell having either the first or second resistance based on the data held by the memory cell which has a

resistance between the first and second resistances.

26. The device according to claim 25, wherein the sense amplifier identifies the data read from the memory cell having either the first or second resistance by a magnitude with respect to the data read from the memory cell which has the resistance between the first and second resistances.

27. The device according to claim 23, further comprising:

a hold circuit which holds the value of the write current required to set the resistance of the magneto-resistive element of the memory cell to a value between the first and second resistances.

28. The device according to claim 23, further comprising:

a judgment circuit to judge whether or not the resistance of the magneto-resistive element of the memory cell is in a predetermined range between the first and second resistances; and

a control circuit to command the rewriting of the data with respect to the memory cell, when the resistance of the magneto-resistive element of the memory cell is not in the predetermined range as a result of judgment in the judgment circuit.

29. The device according to claim 28, wherein the control circuit controls the value of the current supplied by the driver circuit in accordance with a

judgment result in the judgment circuit in commanding the rewriting.

30. A semiconductor memory device comprising:

a plurality of word lines formed along a first direction;

a plurality of first bit line formed along a second direction intersecting at right angles with the first direction;

a second bit line formed along the second direction;

first memory cells arranged at the intersections of the word lines and the first bit lines, each first memory cell including a magneto-resistive element which has either a first resistance or a second resistance smaller than the first resistance;

second memory cells arranged at the intersections of the word lines and the second bit line, each including a magneto-resistive element which has a resistance intermediate between the first and second resistances;

a row decoder which selects the word lines;

a row driver which supplies a first write current to the word lines to set the magneto-resistive elements included in the first memory cells at the first or second resistance and which supplies a second write current to the word lines to set the the magneto-resistive elements included in the second memory cell

to a resistance intermediate between the first and second resistances;

a column selector which selects the first and second bit line;

a column driver which supplies a third write current to the first and second bit lines; and

a sense amplifier which amplifies data read from the first memory cell selected by the row driver and column driver, on the basis of data held in any of the second memory cells.

31. A control method of a semiconductor memory device comprising:

writing first data in a memory cell including a first magneto-resistive element, and writing second data in a reference cell including a second magneto-resistive element, the first magneto-resistive element of the memory cell in which the first data is written having either a first resistance or a second resistance smaller than the first resistance, the second magneto-resistive element of the reference cell in which the second data is written having a resistance between the first and second resistances;

precharging the bit line;

reading the first and second data in the bit line from the memory cell and reference cell; and

amplifying the first data read in the bit line based on the second data.

32. The method according to claim 31, wherein the second data is written into the reference cell at a die sort test time.

33. The method according to claim 31, further comprising:

holding information on a write current required in writing the second data in the reference cell in a hold circuit;

verifying whether or not the second data written in the reference cell is normal after writing the second data in the reference cell; and

reading the information held in the hold circuit and using the write current based on the information to write the second data in the reference cell again, when the second data is judged not to be normal as a result of the verification.

34. The method according to claim 31, further comprising:

verifying whether or not the resistance of the magneto-resistive element of the reference cell is in a predetermined range between the first and second resistances, after writing the second data in the reference cell; and

changing the value of the write current based on the verification result and writing the second data in the reference cell, when the resistance is judged not to be in the predetermined range as the result of the

verification.

35. The method according to claim 31, wherein the memory cell and reference cell are disposed in an intersection of the bit line and the word line crossing at right angles to the bit line, and

an absolute value of the write current supplied to the bit line and word line in writing the second data in the reference cell is smaller than that of the write current supplied to the bit line and word line in reversing the data held in the memory cell to write the first data in the memory cell.

36. The method according to claim 35, wherein the write current supplied to the bit line and word line in writing the second data in the reference cell has a value between a minimum write current necessary for reversing the data held in the memory cell and a maximum write current permitted in non-reversing the data.